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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/748,504	12/26/2000	Koji Hayashi	10449-031001	3357

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EXAMINER	
CHU, KIM KWOK	
ART UNIT	**PAPER NUMBER**
2653	

DATE MAILED: 08/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/748,504	HAYASHI ET AL.	
	Examiner	Art Unit	
	Kim-Kwok CHU	2653	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amendment filed on 3/20/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless -*
> *(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.*

2. Claims 1-6 are rejected under 35 U.S.C. § 102(e) as being anticipated by Tsukihashi (U.S. Patent 6,584,053).

Tsukihashi teaches a recording medium having all of the elements and means as recited in claims 1-6. For example, Tsukihashi teaches the following:

(a) as in claim 1, a data recorder for writing data to a recording medium (Fig. 1; column 3, lines 4-6);

(b) as in claim 1, a buffer memory 12 for temporarily storing data before the data is written to the recording medium (Fig. 1; column 3, lines 58-62);

(c) as in claim 1, a buffer underrun determination circuit 17 connected to the buffer memory, for deciding whether the buffer memory is in a state in which a buffer underrun will occur and whether the buffer memory is in a state

in which a buffer underrun will no longer occur (Fig. 3, lines 8-62);

(d) as in claim 1, a recording controller 18 connected to the buffer memory 12 and the buffer underrun determination circuit 17 (Fig. 1);

(e) as in claim 1, the recording controller 18 controls interruption and restart of data writing based on the determination of the buffer underrun determination circuit 17 (Fig. 1; column 3, lines 65-67; column 4, line 1);

(f) as in claim 1, the recording controller 18 includes an encoder 11 connected to the buffer memory 12, for encoding data which is read from the buffer memory 12 to generate recording data (Fig. 1);

(g) as in claim 1, the recording controller 18 includes a clock generator 21 connected to the encoder 11, for generating a system clock and providing the system clock to the encoder to operate the encoder (Fig. 1);

(h) as in claim 1, the recording controller 18 includes a decoder 4 connected to the clock generator 21, for decoding the data written on the recording medium to generate decoded data (Fig. 1);

(i) as in claim 1, the recording controller 18 includes a system control circuit 16 connected to the encoder 11, the

clock generator 21, and the decoder 4 for deciding whether the encoding of the encoder and the decoding of the decoder are synchronized and starting to write the recording data to the recording medium from the encoder when the encoding of the encoder and the decoding of the decoder are synchronized, subsequent to the interruption of the recording of data (Fig. 1; signal synchronizing circuit 20 synchronizes encoding and decoding, column 4, lines 6-9);

(j) as in claim 1, the clock generator suspends to provide the system clock to the encoder until the decoding catches up with the encoding, when the decoding of the decoder is delayed from the encoding of the encoder (Fig. 1; column 7, lines 13-34);

(k) as in claim 2, the clock generator 21 generates a first system clock in accordance with the decoding of the decoder (Fig. 2; first system clock is the reproducing clock; column 4, lines 23-25);

(l) as in claim 2, the clock generator 21 generates a second system clock based on a reference clock having a predetermined frequency (Fig. 2; column 4, line 25 and 26);

(m) as in claim 2, the clock generator 21 provides the first system clock to the encoder until reaching an interrupted position, and provides the second system clock to the encoder

after reaching the interrupted position (column 6, lines 65-67; column 7, lines 1-34);

(n) as in claim 3, the decoder 4 includes a wobble decoder 6 generates a pit clock based on the decoded data, and the clock generator generates the first system clock based on the pit clock (Fig. 1; column 7, lines 43-45);

(o) as in claim 4, the clock generator 21 includes a phase-locked loop (PLL) circuit 24 connected to the decoder, wherein the PLL circuit generates the first system clock (reproducing clock) and the second system clock (recording clock) and selectively outputs the first and second system clocks (Fig. 2, column 2, lines 42-46);

(p) as in claim 5, the clock generator includes a first PLL circuit connected to the decoder to generate a first system clock (Fig. 2; reproducing clock is the first system clock);

(q) as in claim 5, the clock generator 21 generates a second PLL circuit for generating a second system clock based on a reference clock (Fig. 2, recording clock is the second system clock);

(r) as in claim 5, a clock control circuit 20 connected to the first and second PLL circuits, wherein the clock control circuit selectively provides the first and second system clocks to the encoder (Fig. 2 column 8, lines 25-32);

(s) as in claim 6, a recording unit 1 connected to the encoder 11 to write the recording data to the recording medium (Fig. 1); and

(t) as in claim 6, a reading unit 1 connected to the decoder 4 to read the data written on the recording medium and generate read data (Fig. 1).

3. Claim 7 is rejected under 35 U.S.C. § 102(e) as being anticipated by Tsukihashi (U.S. Patent 6,584,053).

Tsukihashi teaches a recording method having all of the steps as recited in claim 7. For example, Tsukihashi teaches the following:

(a) as in claim 7, encoding data to generate the first encoded data (Fig. 1; encoder 11 encodes input data);

(b) as in claim 7, writing the first encoded data to the recording medium (Fig. 1; optical head 1 writes the encoded data to the medium; column 3, lines 31-33);

(c) as in claim 7, reproducing the data written to the recording medium to generate reproduction data when the writing of the data is interrupted (Fig. 1; decoder 4 generates reproduction data after writing of the data is record on the medium);

(d) as in claim 7, encoding data corresponding to the data written on the recording medium to generate second encoded data (Fig. 1; subcode is added to the first encoded data; column 3, lines 38-43);

(e) as in claim 7, suspending the generation of the second encoded data when the reproduction data is delayed from the second encoded data (Fig. 1; buffer underrun; column 3, lines 58-65); and

(f) as in claim 7, restarting the generation of the second encoded data at the moment when the reproduction data catches up with the second encoded data reach the data at which the writing of data was interrupted (Fig. 1; column 3, lines 65-67, column 4, lines 1-9).

4. Claim 8 is rejected under 35 U.S.C. § 102(e) as being anticipated by Tsukihashi (U.S. Patent 6,584,053).

Tsukihashi teaches a recording method for controlling interruption and restart of a recording medium having all of the steps as recited in claim 8. For example, Tsukihashi teaches the following:

(a) as in claim 8, the data is stored in a buffer memory 12 (Fig. 1);

(b) as in claim 8, generating reproduction data when the writing of data to the recording medium is interrupted by sequentially reading the data recorded on the recording medium prior to the writing interruption (Fig. 1; data buffer underrun decision; column 58-65);

(c) as in claim 8, generating recording data when the recording of the data to the recording medium is interrupted by sequentially reading the data stored in the buffer memory interrupted (Fig. 1; encoder 11 generates recording data from the buffer memory);

(d) as in claim 8, suspending the generation of the recording data when the reproduction data is delayed from the recording data (Fig. 1; buffer underrun effects; column 3, lines 58-65);

(e) as in claim 8, restarting the generating of the recording data when the delayed reproduction data catches up with the recording data (Fig. 1; no buffer underrun); and

(f) as in claim 8, restarting the recording of data at the moment the reproduction of data and the recording data reach the data at which the writing of data was interrupted (Fig. 1; normal recording operation with no buffer underrun).

Prior Art

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Maeda (6,272,084) is pertinent because Maeda teaches an information recording/reproducing having an interruption mode.

Kuroda et al. (6,219,309) is pertinent because Kuroda teaches an information recording/reproducing having an operation resume step.

Ishida et al. (5,680,379) is pertinent because Ishida teaches an information recording/reproducing synchronizing method.

Honda (5,586,093) is pertinent because Honda teaches an information recording/reproducing system having a buffer memory for storing suspended writing data.

6. Any response to this action should be mailed to: Commissioner of Patents and Trademarks Washington, D.C. 20231 Or faxed to:

(703) 872-9306 (for formal communications intended for entry. Or:

(703) 746-6909, (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2021 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-4700.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim CHU whose telephone number is (703) 305-3032 between 9:30 am to 6:00 pm, Monday to Friday.

KC 7/23/04

Kim-Kwok CHU
Examiner AU2653
July 23, 2004

(703) 305-3032

William Korzuch

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